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**UNIVERSITI TUN HUSSEIN ONN MALAYSIA**

**FINAL EXAMINATION  
SEMESTER II  
SESSION 2015/2016**

COURSE NAME : LOGIC SYSTEMS  
COURSE CODE : DAE 21603  
PROGRAMME : 2 DAE  
EXAMINATION DATE : JUNE / JULY 2016  
DURATION : 2 HOURS 30 MINUTES  
INSTRUCTION : ANSWER **FOUR (4)** QUESTIONS  
ONLY

THIS QUESTION PAPER CONSISTS OF **EIGHT (8)** PAGES

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**Q1** (a) State the key difference between flip-flops and latches. (3 marks)

(b) With the aid of truth tables, describe the differences between the following flip-flops :

- (i) RS flip flop
- (ii) JK flip flop
- (iii) D flip flop

(12 marks)

(c) There are **four(4)** primary types of flip-flop,( SR, D, JK and T )

- (i) Show how to create a T flip-flop from JK flip-flop.
- (ii) Show how to create a JK flip-flop from D flip-flop.

(5 marks)

(d) Given J, K, Preset, Clear and Clock input for a JK flip-flop in **Figure Q1(d)**.

- (i) Draw the Q output waveform

(5 marks )

**Q2** (a) Explain briefly two application of flip-flop. (4 marks)

(b) For the circuit in **Figure Q2(b)**:

- (i) State the function of this circuit.
- (ii) Determine the external resistors R1 and R2 to give output frequency of 10kHz and duty cycle of 50% if the external capacitor C is 3nF.

(7 marks)

(c) By using JK flip-flop as a ripple counter to count up counter.

- (i) Draw the circuit diagram.
- (ii) Draw the timing diagram as **Figure Q2(c)**.
- (iii) Modify the circuit to operate as a MOD 5 counter.
- (iv) If the input clock frequency is 10 kHz, determine the output frequency of the MOD 5 counter.

(14 marks)

**Q3** (a) What is the advantages of synchronous counters. (4 marks)

(b) The logic diagram and Dual-In-Line Package for IC 7493 is given in **Figure Q3(b)**. Draw the connections diagrams for the following 7493-based counters and determine the output frequency if the input clock frequency is 200 kHz. Show all steps and label the input clock as well as the outputs.

- (i) MOD 7 counter
  - (ii) MOD 11 counter
- (6 marks)

(c) Design a synchronous counter using JK flip-flop to count 4 digits. The count sequence is 2,0,3,1 and repeat. The JK excitation table is shown in **Table Q3(c)**. Show all steps and the design should include the following :

- (i) State diagram
  - (ii) Circuit excitation table used to determine JK flip-flop inputs.
  - (iii) K-maps used to generate minimal expressions for JK inputs.
  - (iv) Logic circuit.
- (15 marks)

**Q4** (a) Explain the data movement in shift registers. (4 marks)

(b) Determine the number of flip-flops needed to construct a shift register capable of storing :

- (i) a 4-bit binary number
  - (ii) Draw the logic diagram as a serial input/serial output shift register.
- (6 marks)

(c) With the aid of logic circuits and tables showing the sequence of states, describe the differences between a Ring counter and a Johnson counter. (15 marks)

- Q5** (a) Describe **five (5)** basic steps taken to create and load a digital circuit into a PLD. (5 marks)
- (b) Name **three (3)** advantages of constructing a digital circuit prototype using a PLD instead of standard logic devices. (3 marks)
- (c) Several types of architecture are used in PLDs. Draw the block diagram of three common types and describe their differences. (6 marks)
- (d) Use the PLA in **Figure Q5(d)** to implement the following functions. Label all inputs and outputs
- (i)  $F1(W, X, Y) = \sum(1,2,3,5,7)$
  - (ii)  $F2(W, X, Y) = \sum(0,4,6,7)$
- (11 marks)

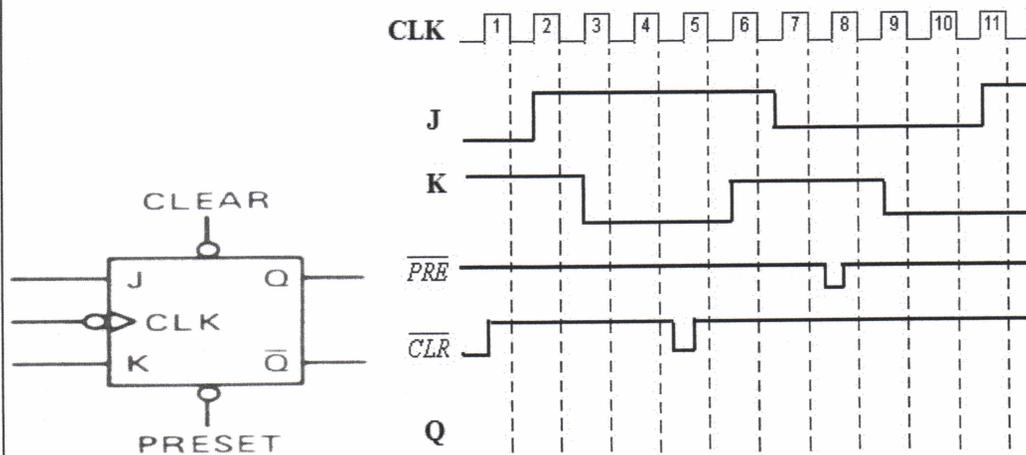
- Q6** (a) **Figure Q6(a)** shows a simplified view of a typical computer system.
- (i) Describe the semiconductor memory devices used.
  - (ii) Explain the differences between the **three (3)** storage devices based on the technology each uses.
  - (iii) Describe the functions of the **three (3)** buses shown. (13 marks)
- (b) A certain memory has a capacity of 4K x 8, determine
- (i) the number of data inputs and data outputs .
  - (ii) the number of address lines.
  - (iii) its capacity in bytes. (6 marks)
- (c) List and describe the **three (3)** major operations in a flash memory. (6 marks)

- END OF QUESTION -

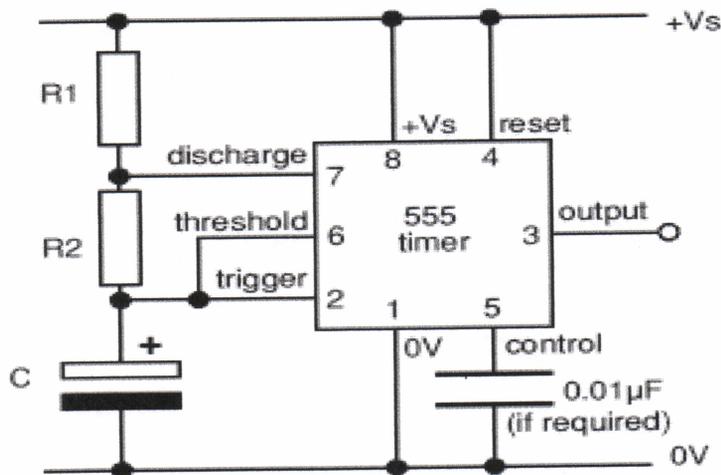
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**FIGURE Q1(d)**

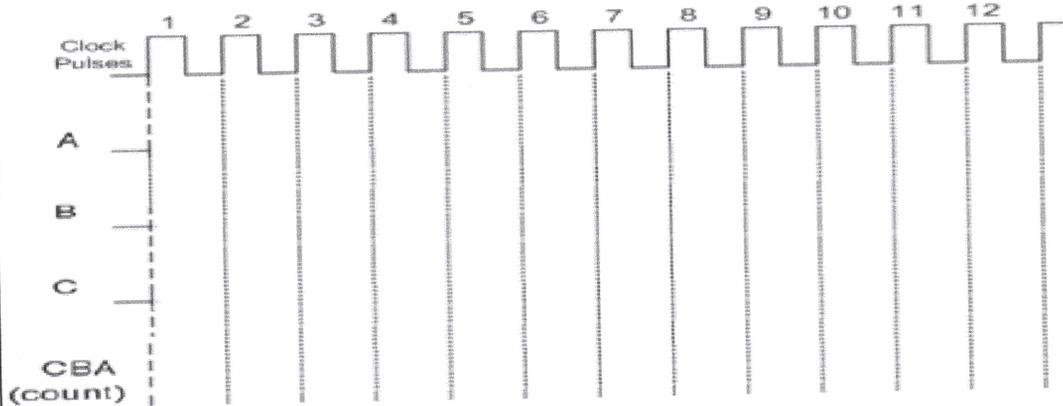


**FIGURE Q2(b)**

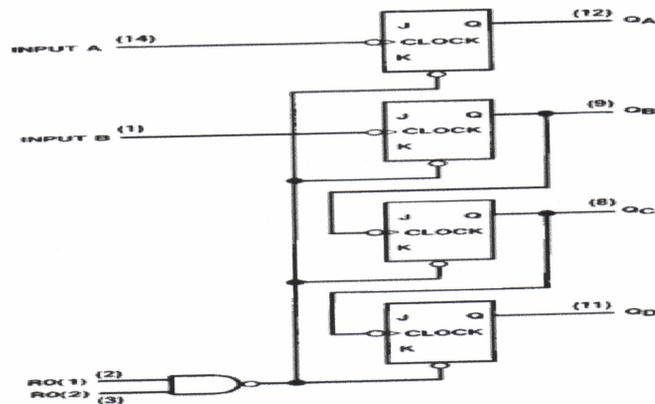
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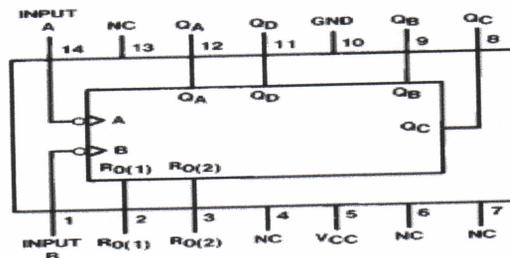
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**FIGURE Q2(c)**



Dual-In-Line Package



**FIGURE Q3(b)**

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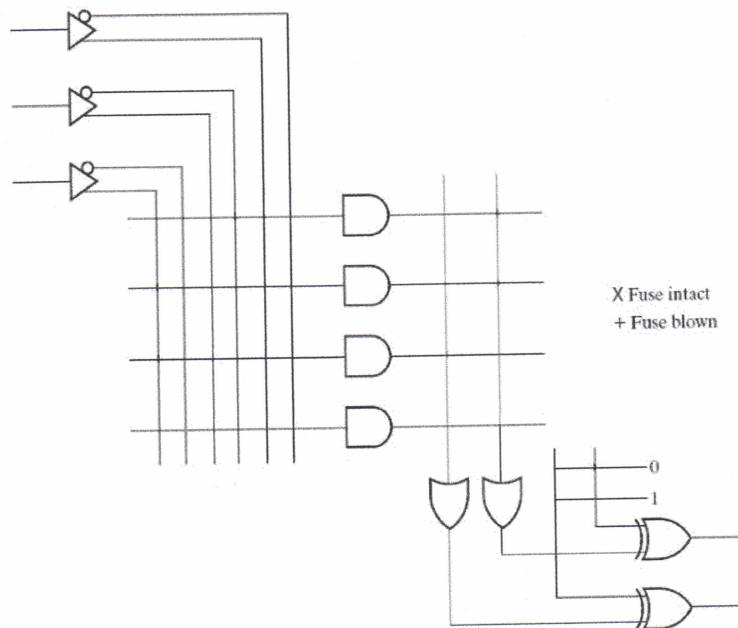
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**TABLE Q3(c): JK Excitation Table**

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

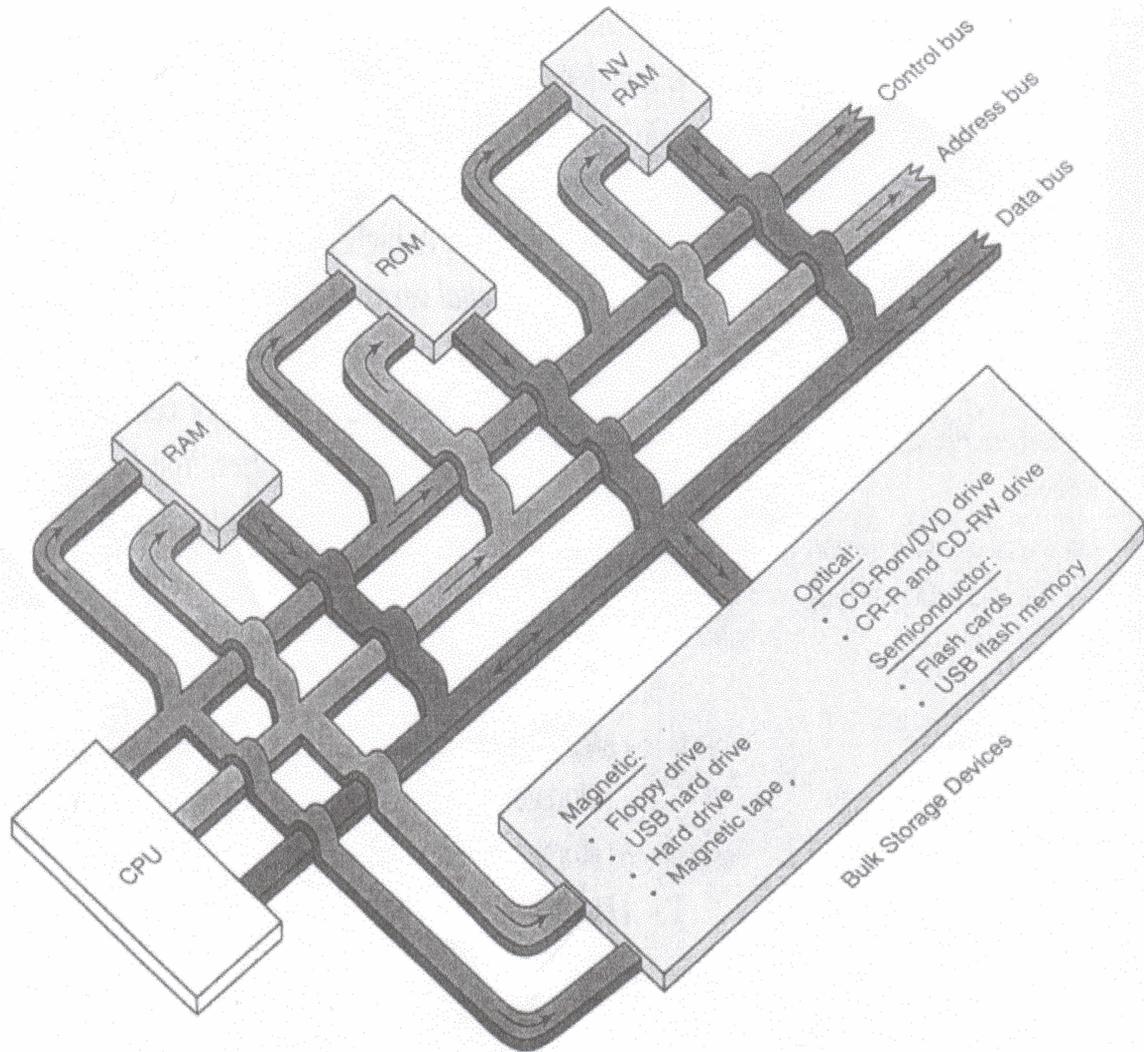


**FIGURE Q5(d)**

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**FIGURE Q6(a)**