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UNIVERSITI TUN HUSSEIN ONN MALAYSIA

**FINAL EXAMINATION
SEMESTER I
SESSION 2013/2014**

COURSE NAME : LOGIC SYSTEM
COURSE CODE : DAE 21603
PROGRAM : 2 DAE
EXAMINATION DATE : DECEMBER 2013/JANUARY 2014
DURATION : 2 ½ HOURS
INSTRUCTION : ANSWER **FOUR (4)** QUESTIONS ONLY

THIS QUESTION PAPER CONSISTS OF **EIGHT (8)** PAGES

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- Q1**
- (a) Explain the operation of an exclusive OR gate. Draw the symbol and build the truth table for its operation. (4 marks)
 - (b) Given J, K, Preset, Clear and Clock input waveform for the JK flip flop in Figure Q1(b). Sketch the Q waveform. (*Attach the Figure Q1(b) with the answer sheet*) (6 marks)
 - (c)
 - (i) Describe a flip-flop.
 - (ii) Differentiate between a latch and a flip-flop.
 - (iii) List out three (3) applications of flip-flop. (5 marks)
 - (d) Illustrate THREE different flip-flops operating in the Toggle mode. (6 marks)
 - (e) Show how to create the following flip flops from JK flip flop:
 - (i) D flip flop
 - (ii) T flip flop (4 marks)
- Q2**
- (a) With the 555 Timer IC and RC component, draw the complete schematic diagram for the operation of monostable (one-shot) and the operation of astable multivibrator. List the operation and function of the 555 pin. (13 marks)
 - (b) Determine the pulse width (t_w) for monostable (One-Shot) if given $E = 9\text{ V}$, $R = 7\text{k}\Omega$ and $C = 2.2\mu\text{F}$. (3 marks)
 - (c) Determine the value of external resistor for a 555 Timer used as an astable multivibrator with output frequency of 15 kHz, $C=0.002\ \mu\text{F}$ and duty cycle of 85%. (9 marks)
- Q3**
- (a) Explain the essential differences between synchronous and asynchronous counters? (4 marks)
 - (b) Fill in the excitation table in **Table Q3(b)**. (*Attach the Table Q3(b) with the answer sheet*) (4 marks)

- (c) Design a synchronous counter using D flip-flops, AND gates and OR gates only, based on the **Table Q3(c)** and the following steps:
- (i) Draw the state transition diagram (4 marks)
 - (ii) Complete the state transition table of the counter (4 marks)
 - (iii) Minimize the D flip-flop input equations using the Karnaugh's Map (4 marks)
 - (iv) Implement the D flip-flop input and draw this synchronous counter. (5 marks)

- Q4** (a) Name four types of registers. (4 marks)
- (b) What is the difference between Johnson Counter and Ring Counter? (1 marks)
- (c) **Figure Q4(c)** shows a bidirectional shift register. The serial input (IN) is HIGH. Assume that initially outputs $Q_0Q_1Q_2Q_3 = 1101$. Do the following if RIGHT/(LEFT) input are HIGH.
- (i) Redraw the 4 flip-flops to show how they are connected by analyzing the combinational logic circuit output. Show all steps. (15 marks)
 - (ii) Complete the timing diagram for outputs Q_0, Q_1, Q_2 and Q_3 (*Attach the Figure Q4(c)(ii) with the answer sheet*) (5 marks)

- Q5** (a) Distinguish between ROM, PROM, EPROM, UV EPROM, EEPROM. (15 marks)
- (b) Explain the difference between the two types of RAM cell? (4 marks)
- (c) A microprocessor uses RAM chips of 1024 x 1 capacity.
- (i) Determine the chips that will be required and calculate the address lines that will be connected to provide capacity of 1024 bytes. (4 marks)
 - (ii) Determine the chips that will be required to obtain a memory of capacity of 16 K bytes. (2 marks)

- Q6** (a) Based on the PLD programming; illustrate the flow of PLD design. (6 marks)
- (b) Several types of architecture are used in PLDs. Draw the block diagram of three common types and describe their differences. (8 marks)
- (c) $F_0(A,B,C,D) = \Sigma m(2, 3, 4, 5, 6, 7, 13, 15)$
 $F_1(A,B,C,D) = \Sigma m(6, 7, 13, 14, 15)$
 $F_2(A,B,C,D) = \Sigma m(4, 5, 6, 13, 14)$

From the above function equation, write the suitable Boolean expressions and then implement these functions using PLA with 5 AND array as shown in **Figure Q6(c)**.
(Attach the **Figure Q6(c)** with the answer sheet)

(11 marks)

-END OF QUESTION-

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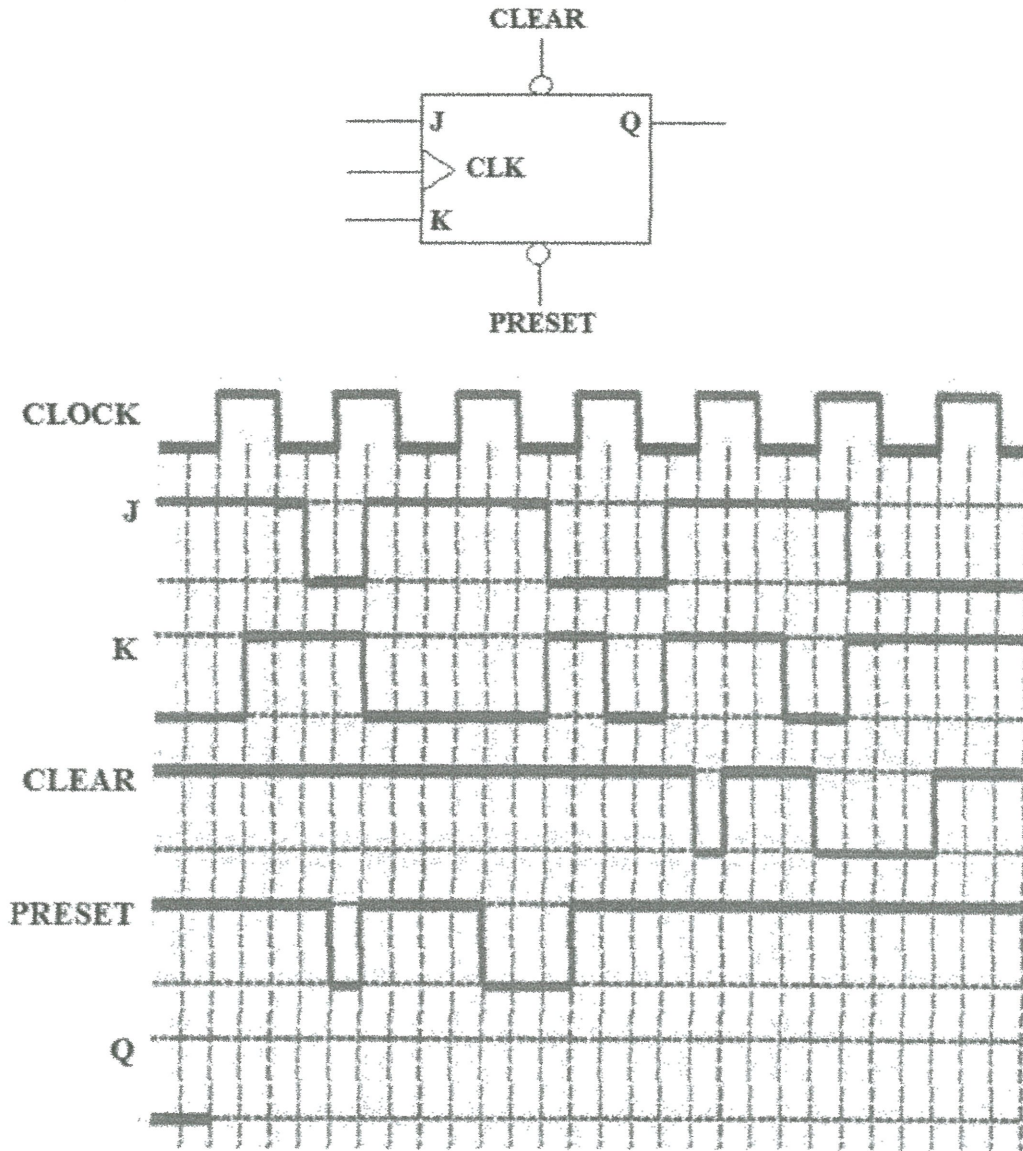


FIGURE Q1(b)

(To be attached with the answer sheet)

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TABLE Q3(b): Excitation table

| Q | Q ⁺ | D FF | T FF | JK FF | |
|---|----------------|------|------|-------|---|
| | | D | T | J | K |
| 0 | 0 | | | | |
| 0 | 1 | | | | |
| 1 | 0 | | | | |
| 1 | 1 | | | | |

(To be attached with the answer sheet)

TABLE Q3(c): Output sequence

| Current active output | Next active output |
|-----------------------|--------------------|
| 0 | 6 |
| 1 | 2 |
| 2 | 5 |
| 5 | 0 |
| 6 | 1 |
| 3 or 4 or 7 | 2 |

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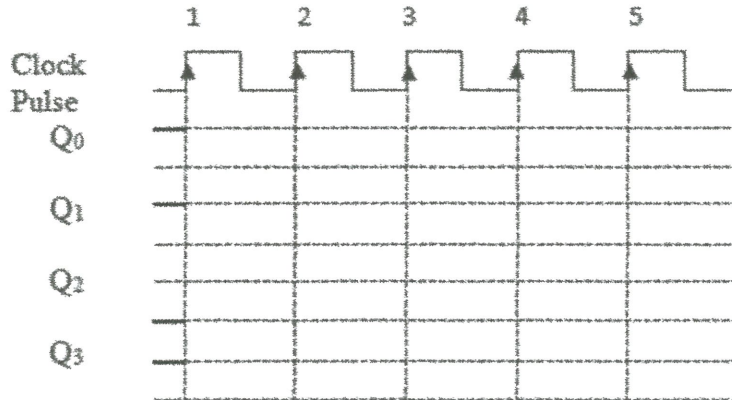


FIGURE Q4(c)(ii)

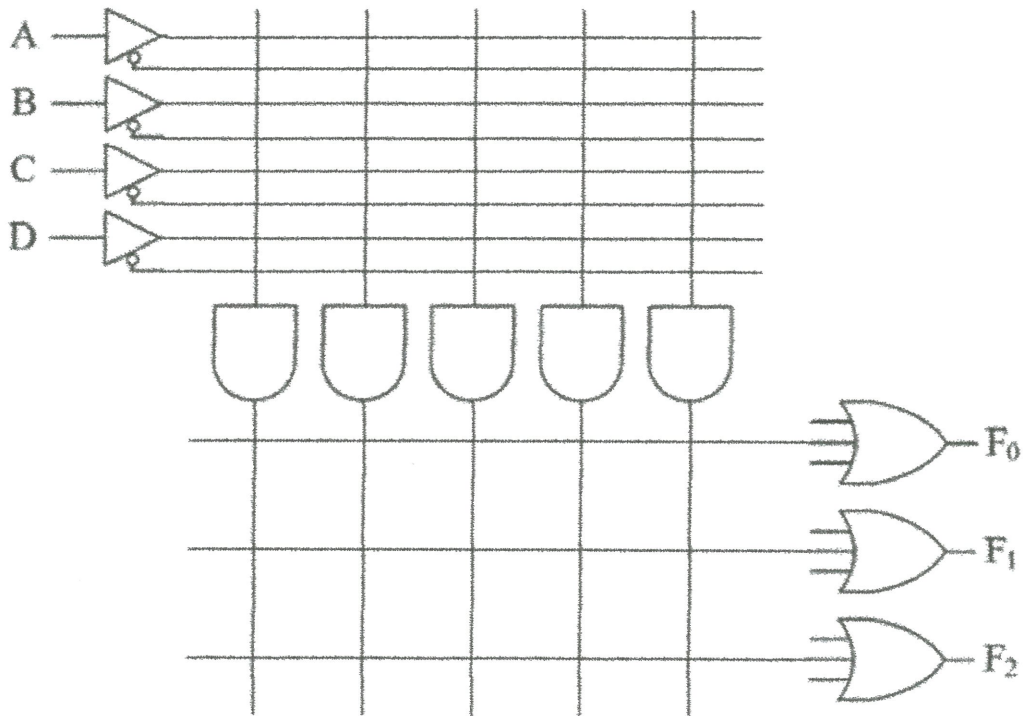


FIGURE Q6(c)

(To be attached with the answer sheet)